AUR6501

3-CHANNEL LED DRIVER with Dimming Control

Features

- 3-channel individual dimming control
- Maximum output current up to 30mA per channel
- Serial-in clock frequency up to 15 MHz
- Built-in buffers for cascading clock, data, latch, and enable
- Internal power-on reset
- Schmitt trigger CMOS logic input
- Power supply voltage: 2.0V ~ 6.0V

Description

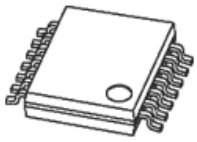
AUR6501 is a 3-channel (R, G, B) LED driver. The chip enables serial data-in and data-out interface with built-in shift registers, internal data latches and output drivers. It is designed ideally for full-color LED decorative or general lighting, signs and display applications.

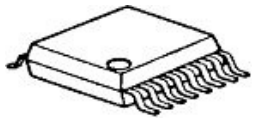
Data, clock, latch, and enable output buffers can be used for cascading with next AUR6501. It is also adapted to control other MOSFETs or LED drivers especially in high power LED applications.

Applications

- LED Decorative Lighting
- LED General Lighting
- Flexible Indoor/Outdoor Video or Sign Displays

Package Information



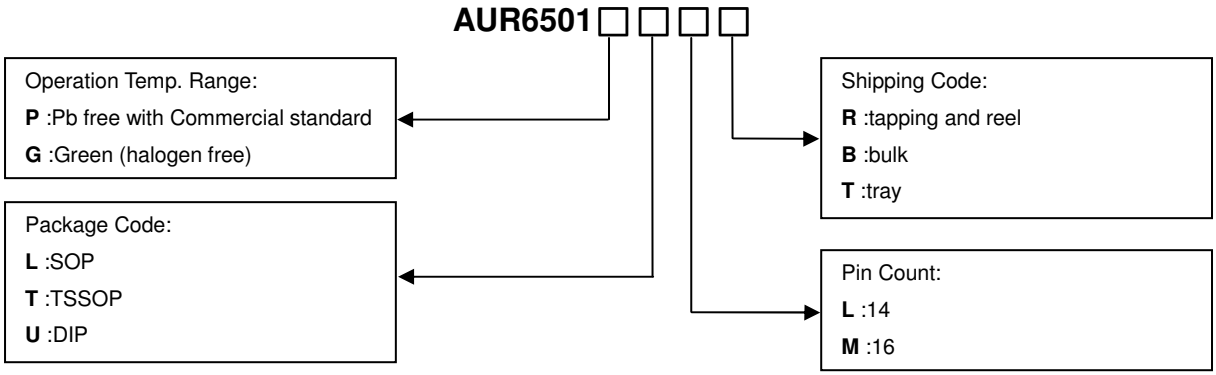


PDIP14 TSSOP14

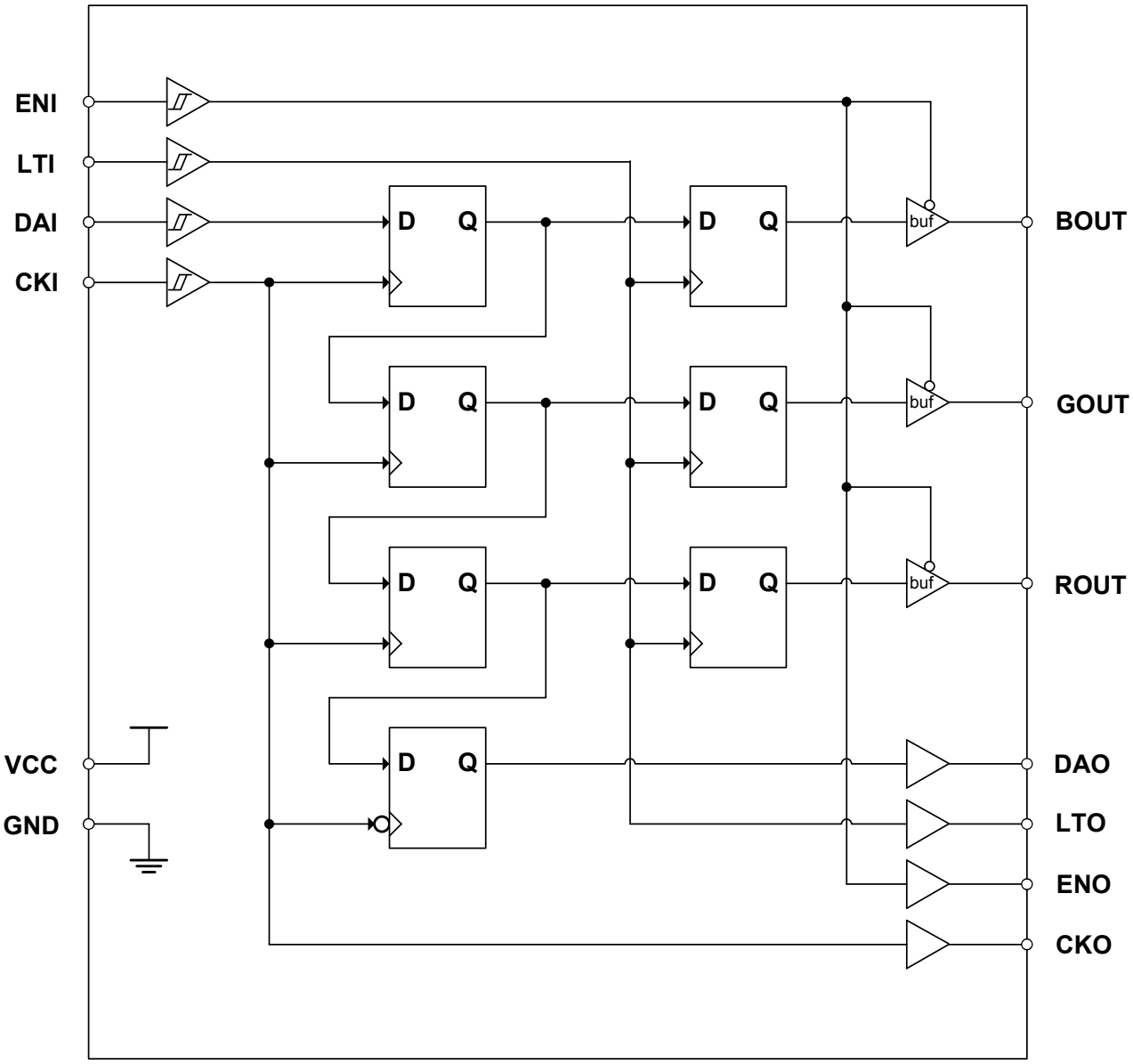
SOP14 TSSOP16

COB

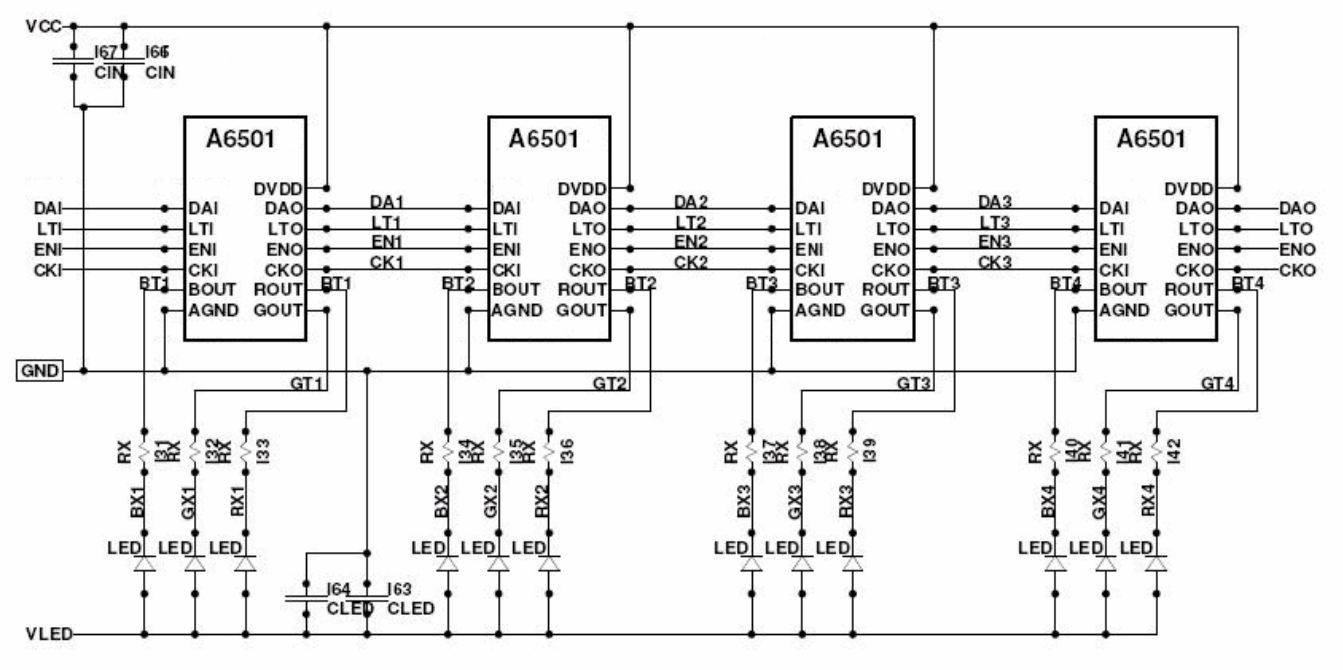
Ordering Information



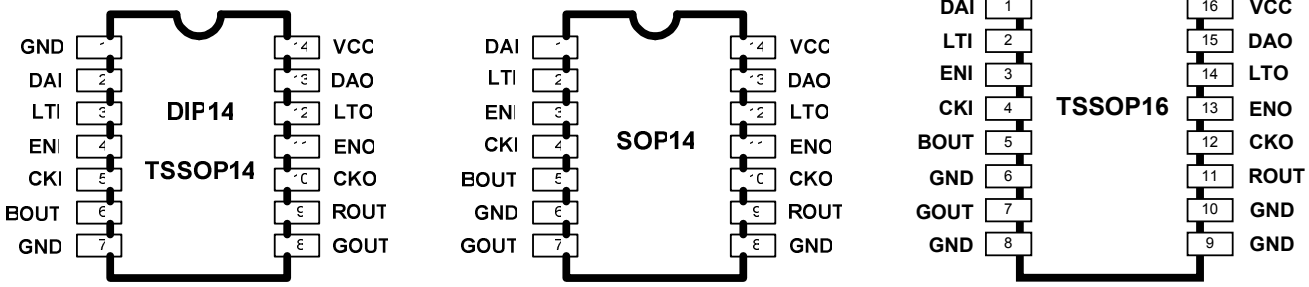
Block Diagram



Application Circuit

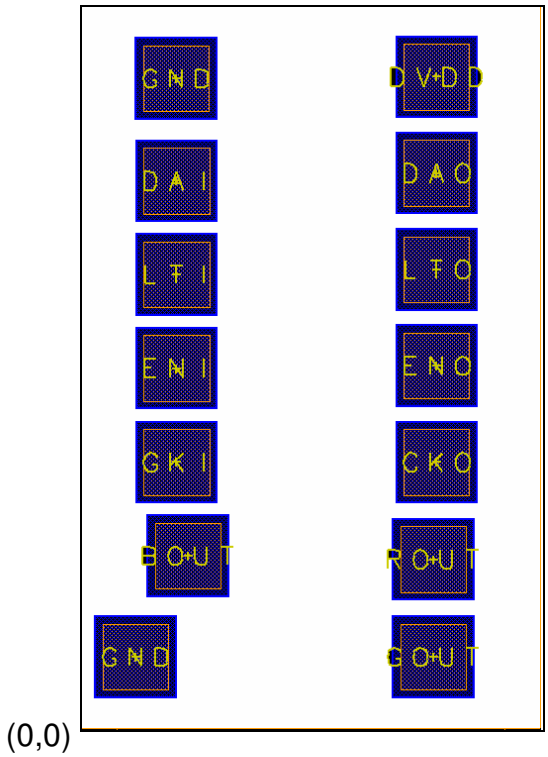


Pin Description



PIN NAME	DIP14 TSSOP14	SOP14	TSSOP16	Pin Type	FUNCTION
GND	1,7	6,8	6,8,9,10	GROUND	Ground Pin
DAI	2	1	1	DI	Serial data input
LTI	3	2	2	DI	Data-input latch pulse, latches data into internal registers at the rising edge of LTI
ENI	4	3	3	DI	Output enable control input Output is turned on when ENI = "**L**", output is high impedance when ENI = "**H**".
CKI	5	4	4	DI	Clock input pin for serial data transfer. Data is sampled at the rising edge of CKI
BOUT	6	5	5	AO	LED dimming control output
GOUT	8	7	7	AO	LED dimming control output
ROUT	9	9	11	AO	LED dimming control output
CKO	10	10	12	DO	Clock output signal
ENO	11	11	13	DO	Enable output signal
LTO	12	12	14	DO	Latch output signal
DAO	13	13	15	DO	Data output signal
VCC	14	14	16	POWER	Power supply voltage input

PAD Diagram



PAD size: 90 x 90 um^2 Die size: 992 x 631 um^2

PIN No.	PIN NAME	Center Coordinate	
		X	Y
1	GND	132.15	877.7
2	DAI	132.15	749.7
3	LTI	132.15	621.7
4	ENI	132.15	493.7
5	CKI	132.15	365.7
6	BOUT	147.85	237.7
7	GND	76.05	99.7
8	GOUT	483.0	99.7
9	ROUT	483.0	232.7
10	CKO	487.5	365.7
11	ENO	487.5	497.2
12	LTO	487.5	628.7
13	DAO	487.5	760.2
14	VCC	487.5	891.7

※ Notice that all GND pin (No.1 and 7) should be bonded to ground.

Maximum Ratings (Ta = 25℃ , Tj(max) = 140℃)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	VCC	- 0.3 ~ 7.0	V
Logic Input Voltage	VIN	- 0.3 ~ VCC+0.3	V
Driver Output Current	IOUT	30	mA
Driver Output Voltage	VOUT	- 0.3 ~ 7.0	V
Input Clock Frequency	FCKI	15	MHz
GND Pin Current	IGND	100	mA
Power Dissipation	PD	tbd (TSSOP16 : Ta=25℃) tbd (TSSOP14 : Ta=25℃) tbd (SOP14 : Ta=25℃) tbd (DIP14 : Ta=25℃)	W
Thermal Resistance	Rth(j-a)	tbd (TSSOP16) tbd (TSSOP14) tbd (SOP14) tbd (DIP14)	℃/W
Operating Temperature	Top	- 40 ~ 85	℃
Storage Temperature	Tstg	- 65 ~ 150	℃

Recommended Operating Condition

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	VCC		2.0	5.0	6.0	V
Driver Output Voltage	VOUT	Driver Off			6.0	
Output Current	IOUT	(Driver) OUT (R, G, B)			30	mA
	IOH	(Logic) SERIAL-OUT			1.0	
	IOL				-1.0	
Logic Input Voltage	VIH	VCC = 3.0V ~ 5.5V	0.8VCC		VCC	V
	VIL		GND		0.2VCC	
CKI Pulse Width	twCKI	VCC = 3.0V ~ 5.5V	25			ns
Set-up Time of DAI	tsetup(D)		10			
Hold Time of DAI	thold(D)		10			
Set-up Time for LTI	tsetup(L)		20			

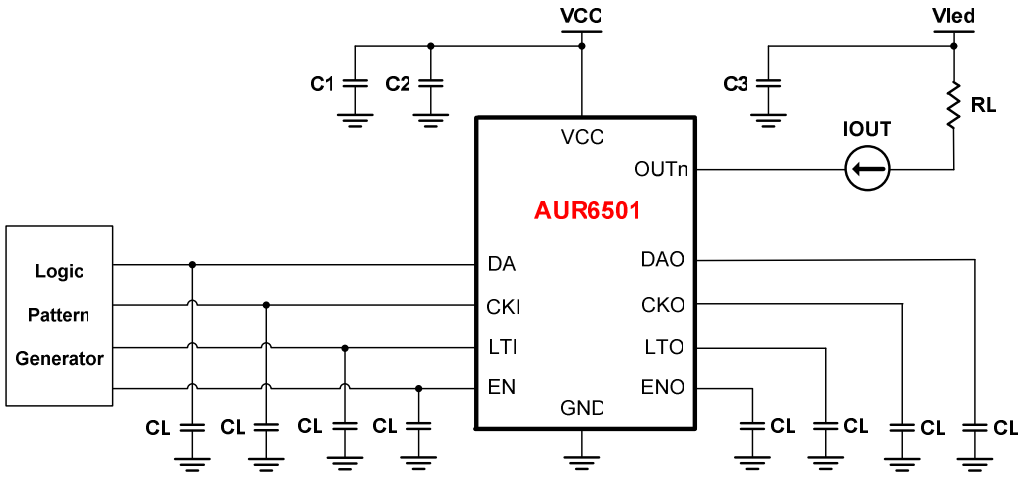
Electrical Characteristics(VCC = 5.0V, Ta = 25℃ , Tj(max) = 140℃)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Logic Input Voltage 'H' Level	VIH	CMOS logic level	0.8VCC		VCC	V
Logic Input Voltage 'L' Level	VIL		GND		0.2VCC	
Driver Output Leakage Current	IOL	VOH = 6.0V			1.0	μA
Logic Output Voltage (S-OUT)	VOL	IOL = 1mA			0.2	V
	VOH	IOH = -1mA	VCC-0.2			
Supply Current	IDD_DC	EN = VCC DC measurement		1		uA

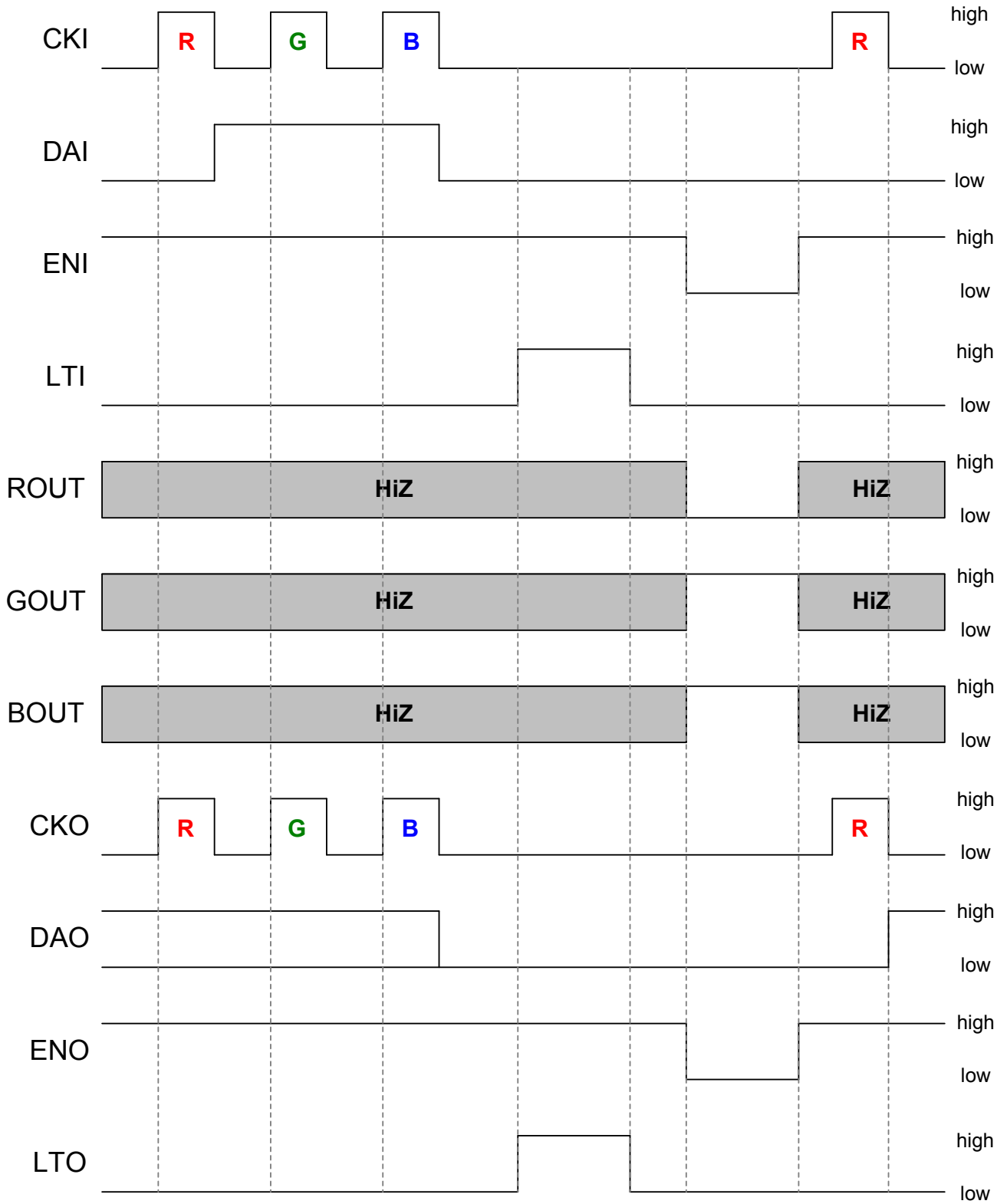
Switching Characteristics(Ta = 25℃ , Tj(max) = 140℃)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay (**L→H**): CKI to CKO	tpLH(C)	VCC=5.0V VIH=VCC VIL=GND RL=51Ω Vled=5.0V CL=15pF C1=1uF C2=0.1uF C3=4.7uF		10		ns
Propagation Delay (**H→L**): CKI to CKO	tpHL(C)			10		
CKO to DAO	td(D)			10		
Propagation Delay (**L→H**): LTI to LTO	tpLH(L)			10		
Propagation Delay (**H→L**): LTI to LTO	tpHL(L)			10		
Propagation Delay (**L→H**): ENI to ENO	tpLH(E)			10		
Propagation Delay (**H→L**): ENI to ENO	tpHL(E)			10		
Propagation Delay (**L→H**): LTI to OUTn	tpLH(LO)			20		
Propagation Delay (**H→L**): LTI to OUTn	tpHL(LO)			20		
Propagation Delay (**L→H**): ENI to OUTn	tpLH(EO)			20		
Propagation Delay (**H→L**): ENI to OUTn	tpHL(EO)			20		
Rise Time of OUTn	tor			100		
Fall Time of OUTn	tof			100		

Switching Test Diagram



Timing Diagrams

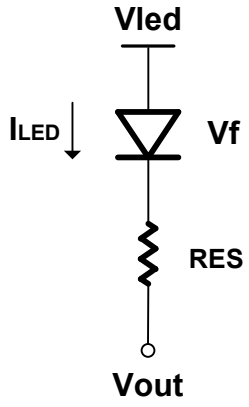


Setting LED Current

The output current level of individual driver is established by an external resistor RES for each channel. The value of external resistor setting LED current can be determined by the equation below. It is recommended the voltage at driver output ports should be as low as possible for consideration of power dissipation and to keep Vled stable for operating LED in constant current.

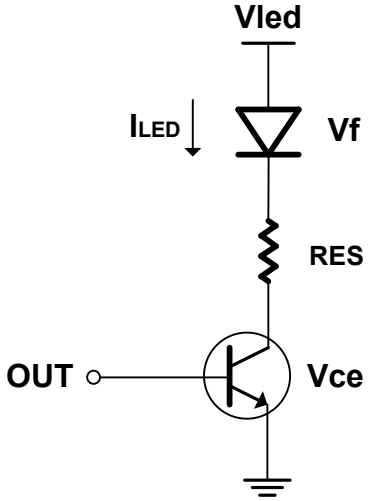
Typical Application #1

$$RES\ (\Omega) = [\ Vled(V) - Vf(V) - Vout(V)\ ] / I_{LED}(A)$$

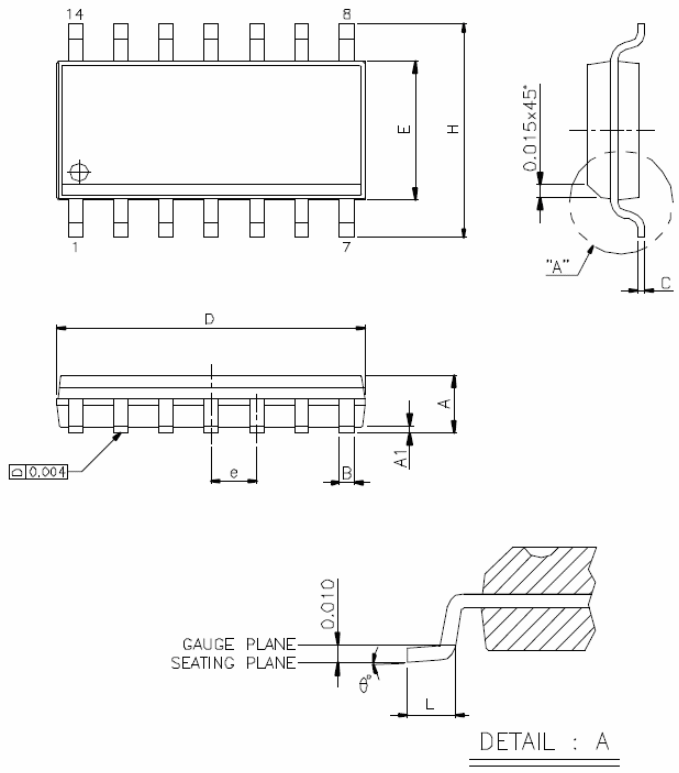


Typical Application #2

$$RES\ (\Omega) = [\ Vled(V) - Vf(V) - Vce(V)\ ] / I_{LED}(A)$$



◎ AUR6501 Package Specification – SOP14 Outline Drawing

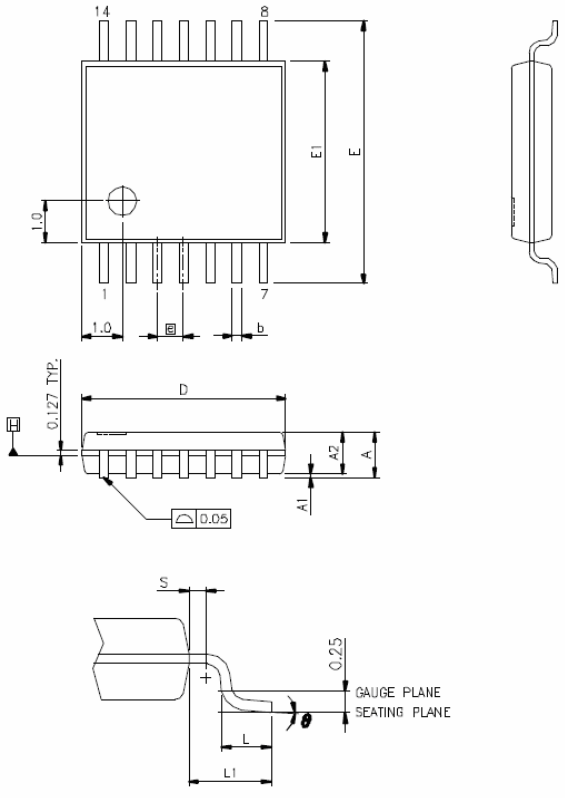


SYMBOLS	MIN.	NOM.	MAX.
A	0.058	0.064	0.068
A1	0.004	–	0.010
B	0.013	0.016	0.020
C	0.0075	0.008	0.0098
D	0.336	0.341	0.344
E	0.150	0.154	0.157
e	–	0.050	–
H	0.228	0.236	0.244
L	0.015	0.025	0.050
θ°	0°	–	8°

UNIT : INCH

NOTES:
1.JEDEC OUTLINE : MS-012 AB
2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3.DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

◎ AUR6501 Package Specification – TSSOP14 Outline Drawing

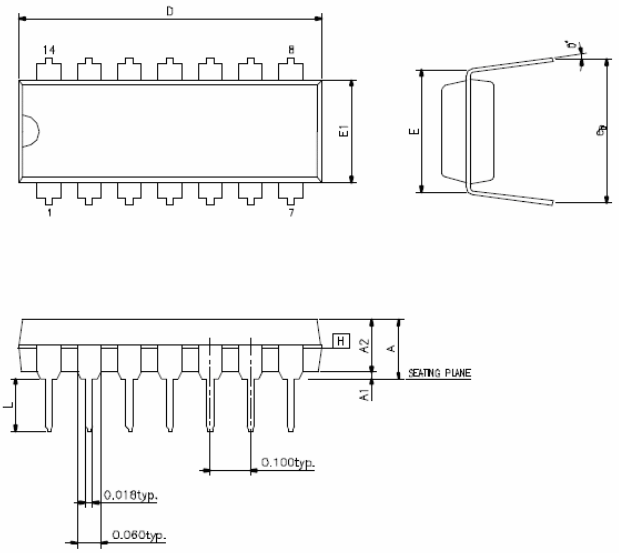


VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.50	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

NOTES:
1.JEDEC OUTLINE : MO-153 (AB-1)
2.DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
3.DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
4.DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM.
5.DIMENSIONS 'D' AND 'E1' TO BE DETERMINED AT DATUM PLANE H .

◎ AUR6501 Package Specification – PDIP14 Outline Drawing

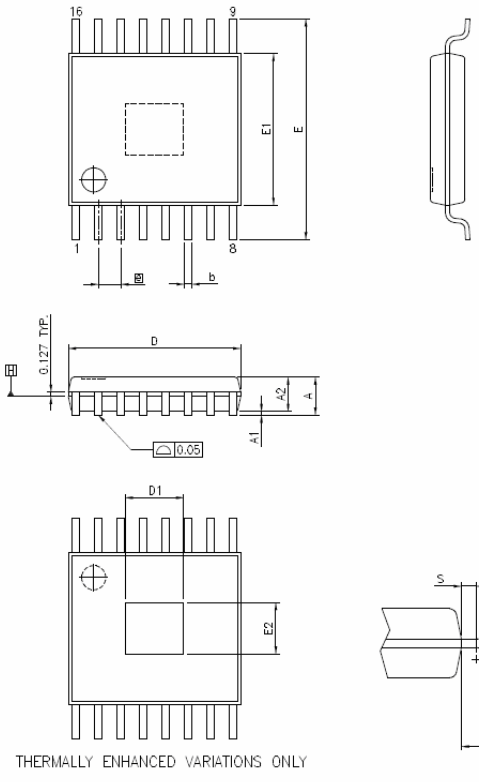


SYMBOLS	MIN.	NOR.	MAX.
A	–	–	0.210
A1	0.015	–	–
A2	0.125	0.130	0.135
D	0.735	0.750	0.775
E		0.300 BSC.	
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
e_B	0.335	0.355	0.375
θ°	0	7	15

UNIT : INCH

NOTES:
1. JEDEC OUTLINE : MS-001 AA
2. "D","E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH.
3. eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
4. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
5. DISTANCE BETWEEN LEADS INCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MININUM.
6. DATUM PLANE H COINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.

◎ AUR6501 Package Specification – TSSOP16 Outline Drawing



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.00	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E		6.40 BSC	
e		0.65 BSC	
L1		1.00 REF	
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

⚠ THERMALLY ENHANCED DIMENSIONS(SHOWN IN MM)

PAD SIZE	E2		D1	
	MIN.	MAX.	MIN.	MAX.
118X11E	2.40	3.00	2.40	3.00

NOTES:
1. JEDEC OUTLINE : MO-153 AB/MO-153 ABT(THERMALLY ENHANCED VARIATIONS ONLY)
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
3. DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
4. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM.
5. DIMENSIONS "D" AND "E1" TO BE DETERMINED AT DATUM PLANE H .