Dual High-Efficiency PWM Step-Down DC-DC Converter

Features

- Dual Channel High efficiency Buck Power Converter
- Low Quiescent Current
- 1A Output Current
- Adjustable Output Voltage from 1V to 3.3V
- Wide Operating Voltage Ranges : 2.5 V to 5.5 V
- Built-in Power Switches for Synchronous Rectification with high Efficiency
- 600mV Feedback Voltage
- 1.5MHz Constant Frequency Operation
- Automatic PWM/LDO Mode switching control
- Thermal Shutdown protection
- Low Drop-out Operation at 100% Duty-Cycle
- No Schottky Diode Required

Applications

- Mobile Phones, Digital Cameras and MP3 Players
- Headsets, Radios and other Hand-Held Instruments
- Post DC-DC Voltage Regulation
- PDA and Notebook Computers

Description

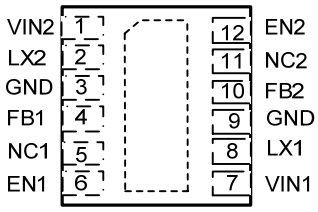
AUR9706 is a high efficiency step-down DC-DC voltage converter. The chip operation is optimized using constant frequency, peak-current mode architecture with built-in synchronous power MOS switchers and internal compensators to reduce external part counts. It is automatically switching between the normal PWM mode and LDO mode to offer improved system power efficiency covering a wide range of loading conditions.

The oscillator and timing capacitors are all built-in providing an internal switching frequency of 1.5MHz that allows the use only small surface mount inductors and capacitors for portable product implementations.

Additional features included integrated soft-start (SS), under-voltage-lock-out (UVLO) and thermal shutdown detection (TSD) to provide reliable product applications.

The device is available in adjustable output voltage versions ranging from 1V to 3.3V, and is able to deliver up to 1A.

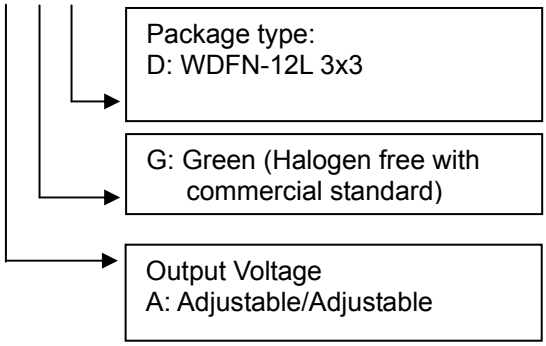
Package Information



WDFN – 12L (3x3)

Order Information

AUR9706☐☐☐



Typical Application Circuits

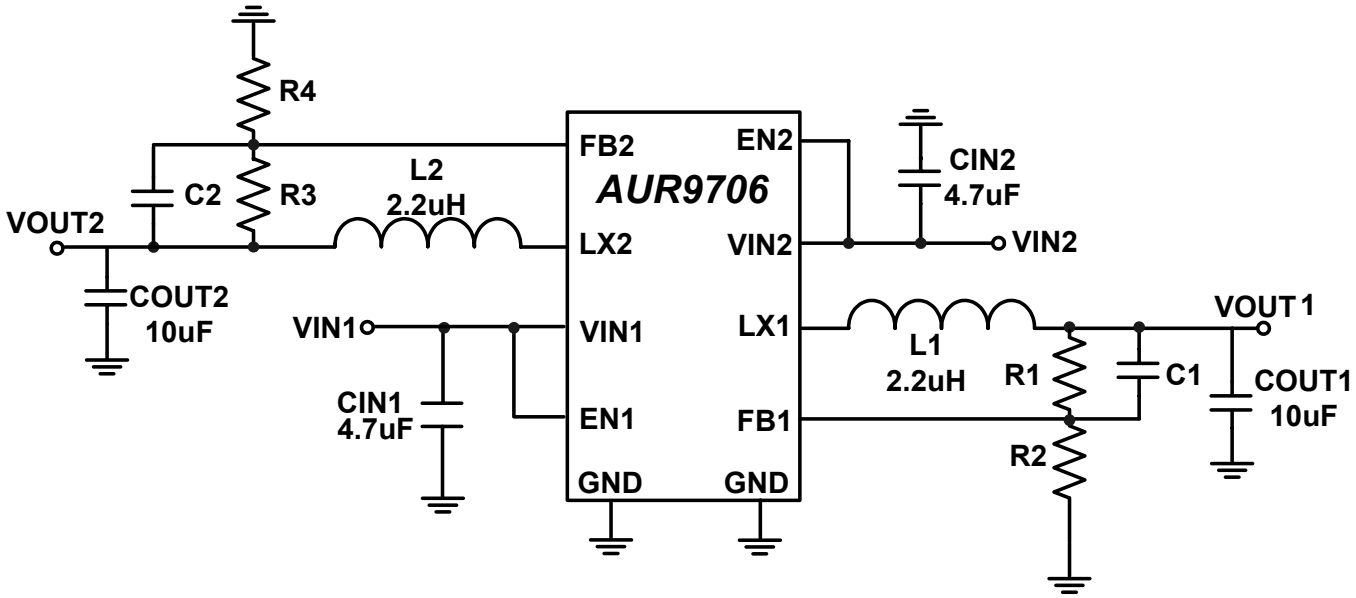


Figure 1. Adjustable Voltage Regulator

$$V_{OUT1} = V_{REF} \times (1 + \frac{R_1}{R_2}) \quad ; \quad V_{OUT2} = V_{REF} \times (1 + \frac{R_3}{R_4})$$

With R2 or R4 = 300 KΩ to 60 KΩ so the I_{R2} or I_{R3} = 2uA to 10uA

And (R1 x C1 or R3 x C2) should be in the range between 3×10^{-6} and 6×10^{-6} for component selection

VOUT1 or VOUT2	R1(kΩ) or R3	R2(kΩ) or R4	C1(pF) or C2	L1(uH) or L2
3.3V	240	53	20	2.2
2.5V	240	75	20	2.2
1.8V	240	120	20	2.2
1.5V	240	160	20	2.2
1.2V	240	240	20	2.2
1.0V	240	300	20	2.2

Table 1. Component guide

Pin Functions

Pin No.	Pin Name	Pin Function
1	VIN2	Power supply input of channel 2
2	LX2	Connection from power MOS of channel 2 to Inductor
3,9	GND	This pin is the GND reference for the NMOS power stage. It must be connected to the system ground.
4	FB/VOUT1	Feedback voltage of channel 1.
5,11	NC1,NC2	No Internal Connect (Floating or Connecting to GND)
6	EN1	Enable Signal Input of channel 1, Active High.
7	VIN1	Power supply input of channel 1
8	LX1	Connection from power MOS of channel 1 to Inductor
10	FB/VOUT2	Feedback voltage of channel 2.
12	EN2	Enable Signal Input of channel 2, Active High.

Maximum Ratings

Characteristic	Symbol	Rating	Unit
Supply Input Voltage	VIN	0~7.0	V
Enable Input voltage	VI	-0.3~VIN+0.3	V
Output Voltage	VOUT	-0.3~VIN+0.3	V
Bypass Pin Voltage	VBP	-0.3~VIN+0.3	V
Power Dissipation, WDFN-12L 3x3 (on PCB, Ta=30°C)		4.35	W
Thermal resistance, WDFN-12L 3x3 (simulation)	θ_{JA}	29.87	°C/W
Thermal resistance, WDFN-12L 3x3 (simulation)	θ_{JC}	52.25	°C/W
Operating junction temperature		160	°C
Operating temperature		-40~+85	°C
Storage temperature		-55~+150	°C

Recommended Operating Condition

Characteristic	Symbol	Rating	Unit
Supply Input Voltage	V_{IN}	2.5 ~ 5.5	V
Junction Temperature Range		-40 ~ 125	°C
Ambient Temperature Range		-40 ~ 80	°C

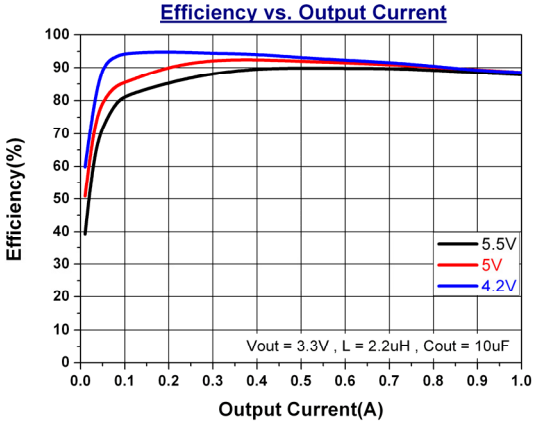
Electrical Characteristics

(Vin=3.6V, Vout=2.5V, Vref=0.6V, L=2.2uH, Cin=4.7uF, Cout=10uF, Ta=25℃, Imax=1A)

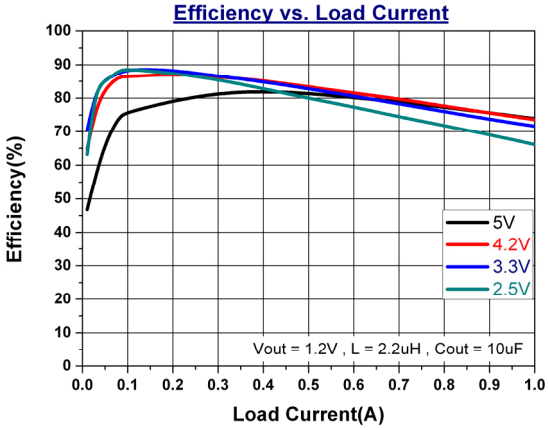
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Input voltage Range	Vin		2.5		5.5	V
Shutdown Current	Ioff	EN=0		0.1	1	uA
Regulated Feedback voltage	VFB	For adjustable output voltage	0.585	0.6	0.615	V
Regulated Output Voltage	Vout	Vin=2.5V to 5.5V Iout=0mA to 1000mA	-3		+3	%
Peak Inductor Current	I_{PK}	Vin=3V, $V_{FB}=0.5V$ or Vout=90%, Duty Cycle<35%		1.5		A
Oscillator Frequency	fosc	Vin=3.6	1.2	1.5	1.8	MHz
PMOSFET Ron	Ron(P)	Vin=3.6, Iout=200mA		0.28		Ω
NMOSFET Ron	Ron(N)	Vin=2.5, Iout=200mA		0.38		Ω
Input DC Bias Current	I_S	Vin=3.6, Iout=200mA		0.25		uA
		Vin=2.5, Iout=200mA		0.35		
LX leakage	I_{LX}	$V_{FB}=0.5V$ or $V_{OUT}=90\%$, $I_{LOAD}=0A$		100		uA
		Ven=0, VLX=0V, 5V, VIN=5V		0.01	0.1	
Feedback Current	Ifb				30	nA
En Leakage Current	Ien			0.01	0.1	uA
En High-Level Input Voltage	VenH	Vin=2.5V ~ 5.5V	1.5			V
En Low-Level Input Voltage	VenL	Vin=2.5V ~ 5.5V			0.6	V
Under Voltage Lock Out				1.8		V
Hysteresis				0.1		V
Thermal Shutdown	Tsd			150		℃

Typical Performance Characteristics

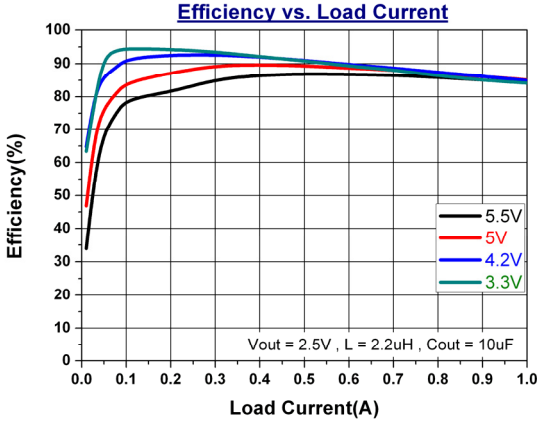
Efficiency vs. Output Current



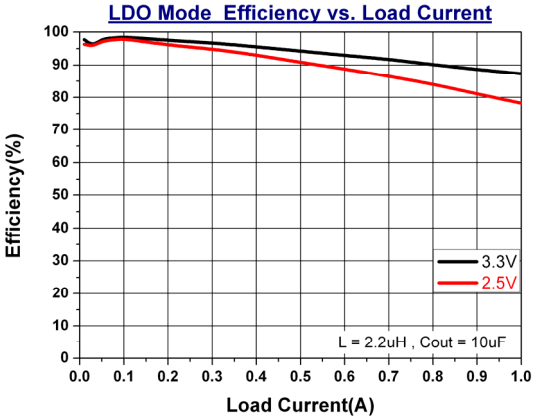
Efficiency vs. Load Current



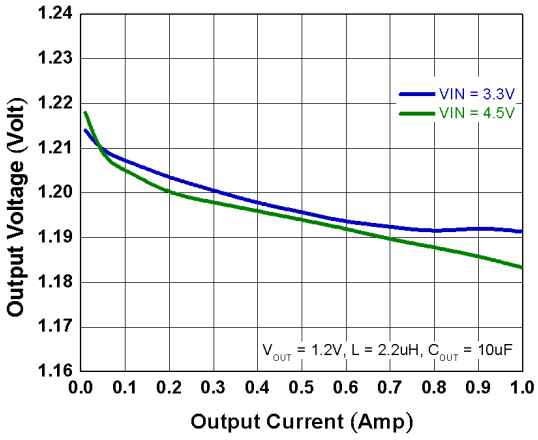
Efficiency vs. Load Current



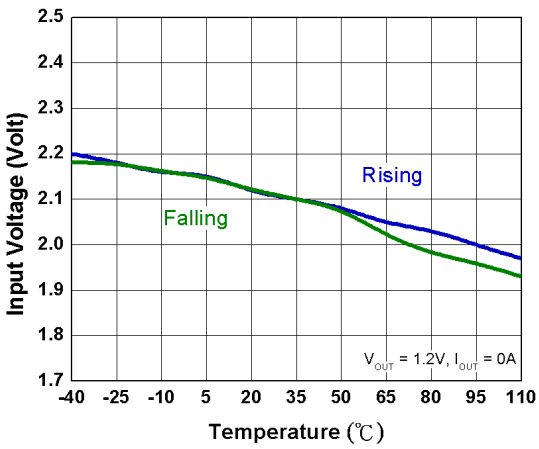
LDO Mode Efficiency vs. Load Current



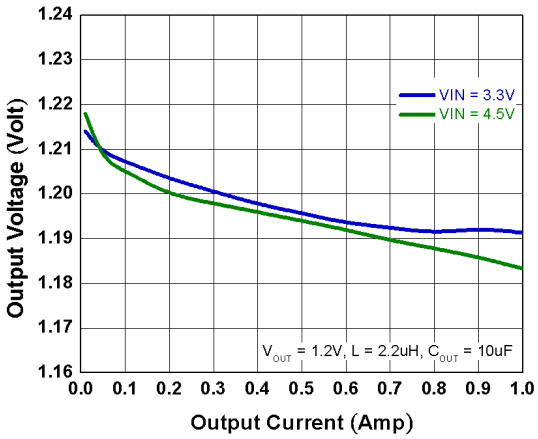
Output Voltage vs Output Current



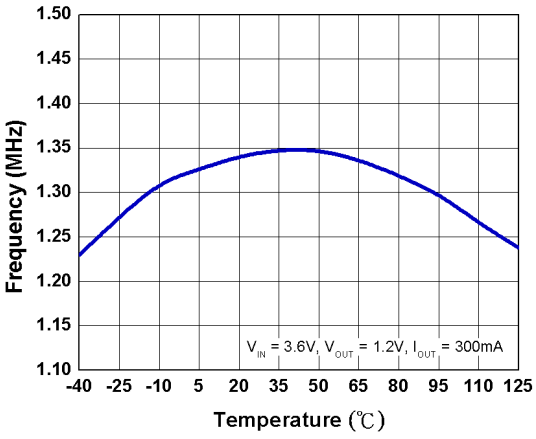
UVLO Threshold vs Temperature



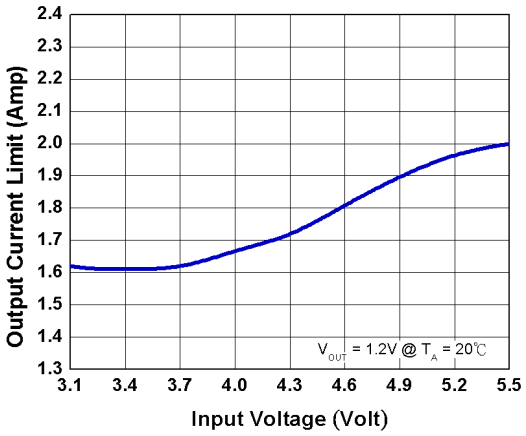
Output Voltage vs Output Current



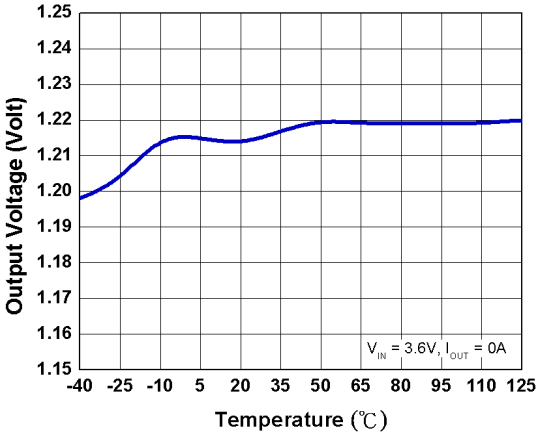
Frequency vs Temperature



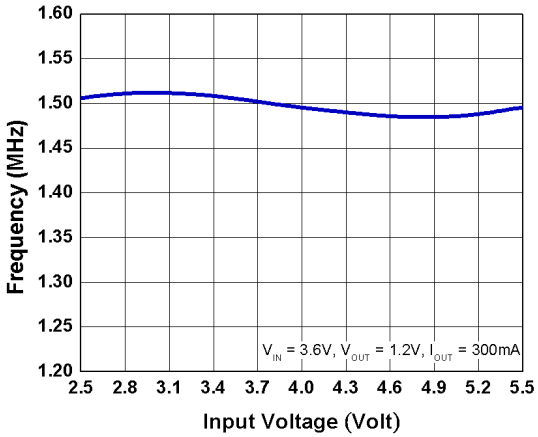
Output Current Limit vs Input Voltage



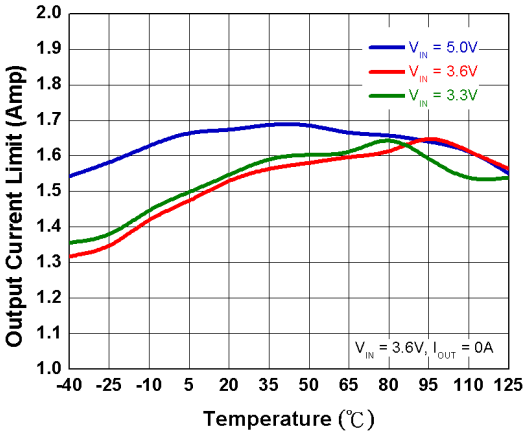
Output Voltage vs Temperature

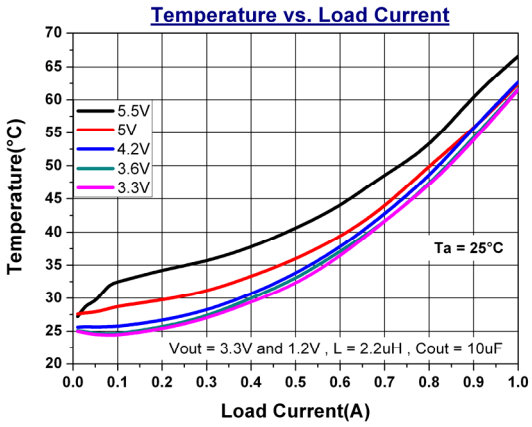


Frequency vs Input Voltage

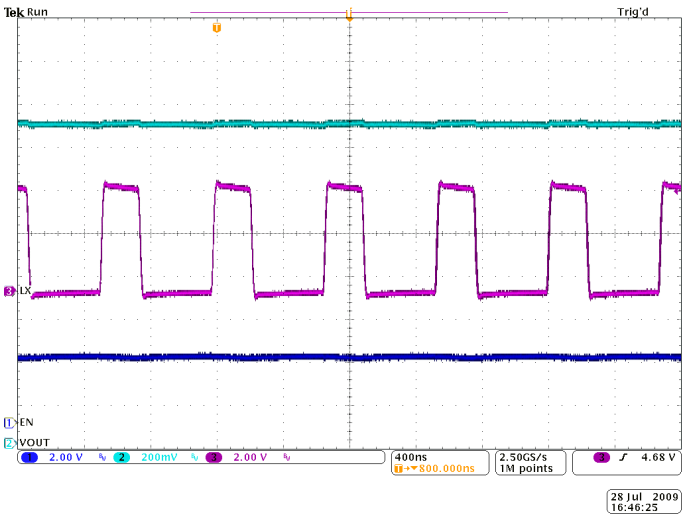


Output Current Limit vs Temperature

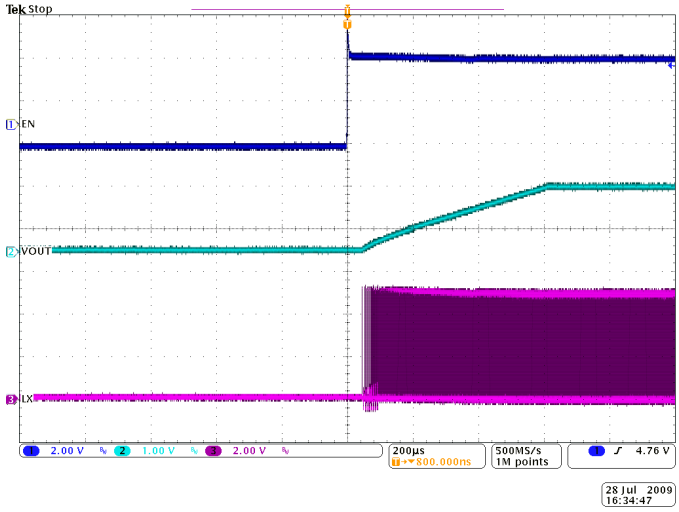




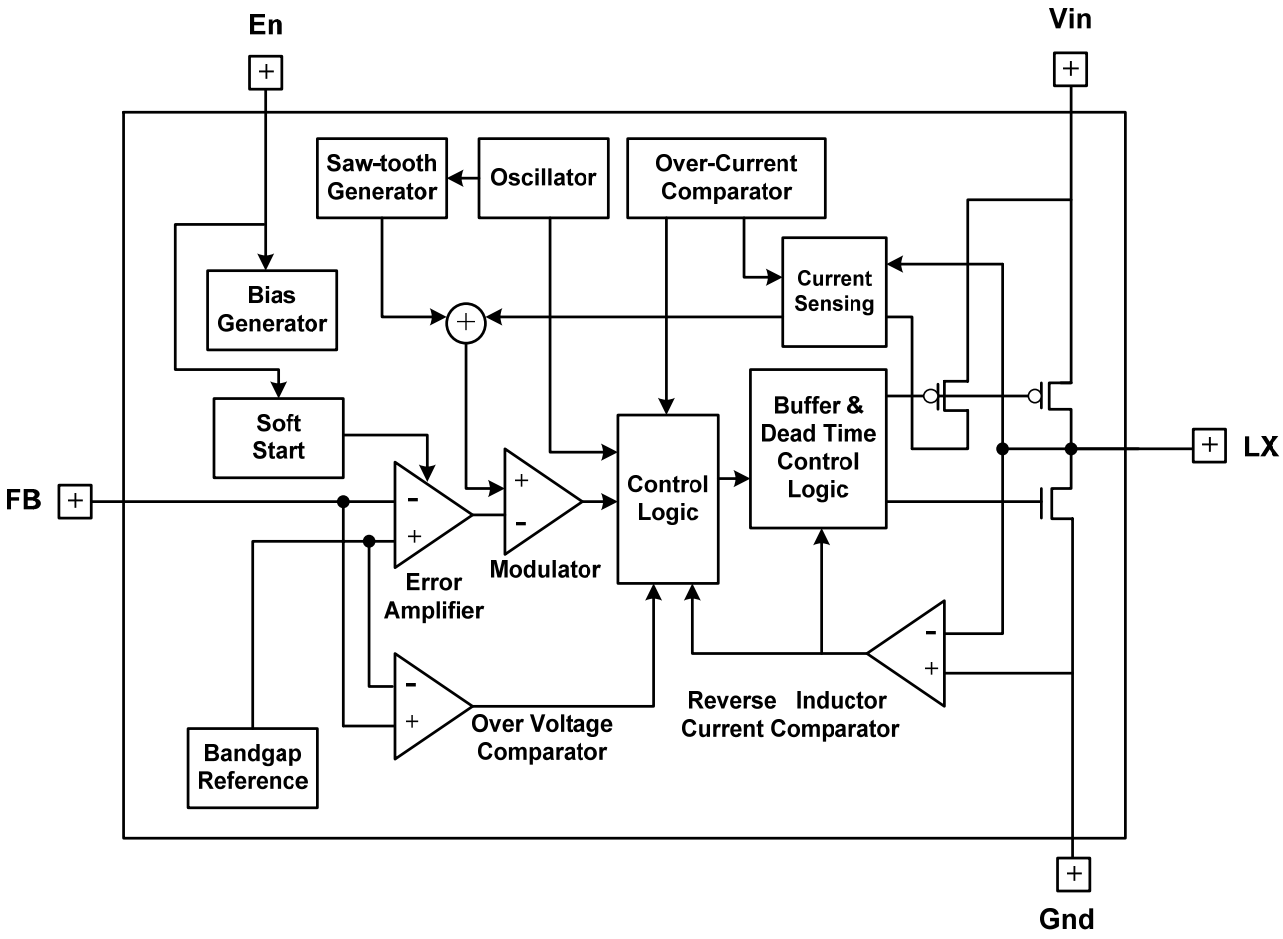
Waveform of V_{IN} =4.5V, V_{OUT} =1.5V, L=2.2uH



Soft start function



Block Diagram



Application Information

The basic AUR9706 application circuits are shown as in Figure 1, External components selection is determined by the load current and is critical with the selection of inductor and capacitor values.

Inductor Selection

For most applications, the value of inductor is chosen based on the required ripple current with the range of 2.2uH to 4.7uH

$$\Delta I_L = \frac{1}{f \times L} V_{OUT}(1 - \frac{V_{OUT}}{V_{IN}})$$

The largest ripple current occurs at the highest input voltage. Having a small ripple current reduces the ESR loss in the output capacitor and improves the efficiency. The highest efficiency is realized at low operating frequency with small ripple current. However, the larger value inductors will be required. A reasonable starting point for ripple current setting is $\Delta I_L = 40\% I_{MAX}$. For a maximum ripple current stays below a specified value , the inductor should be chosen according to the following equation:

$$L = [\frac{V_{OUT}}{f \times \Delta I_L (max)}][1 - \frac{V_{OUT}}{V_{IN}(max)}]$$

The DC current rating of the inductor should be at least equal to the maximum output current plus half the highest ripple current to prevent inductor core saturation. For better efficiency, the lower DC-resistance inductor should be selected

Capacitor Selection

The input capacitance, C_{IN}, is needed to filer the trapezoidal current at the source of the top MOSFET. To prevent the large ripple voltage, a low ESR input capacitor sized for the maximum RMS current must be used . The maximum RMS capacitor current is given by:

$$I_{RMS} = I_{OMAX} \times \frac{[V_{OUT}(V_{IN} - V_{OUT})]^{\frac{1}{2}}}{V_{IN}}$$

It indicates a maximum value at Vin=2Vout, where $I_{RMS} = I_{OUT}/2$. This simple worse-case condition is commonly used for design because even significant deviations do not much relief. The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize output voltage ripple and load step transients, as well as the amount of bulk capacitor that is necessary to ensure the control loop is stable. Loop stability can be also checked by viewing the load step transient response as described in a latter section. The output ripple, ΔV_{OUT} , is determined by:

$$\Delta V_{OUT} \le \Delta I_L [ESR + \frac{1}{8 \times f \times C_{OUT}}]$$

The output ripple is the highest at the maximum input voltage since ΔI_L increase with input voltage.

Load Transient

A switching regulator typically takes several cycles to respond to the load current step. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $(\Delta I_{LOAD} \times ESR)$, where ESR is the effective series resistance of output capacitor. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During the recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

Output Voltage Setting

The output voltage of AUR9706 can be adjusted by a resistive divider according to the following formula:

$$V_{OUT} = V_{REF} \times (1 + \frac{R_1}{R_2}) = 0.6V \times (1 + \frac{R_1}{R_2})$$

The resistive divider senses the fraction of the output voltage as shown in Figure2.

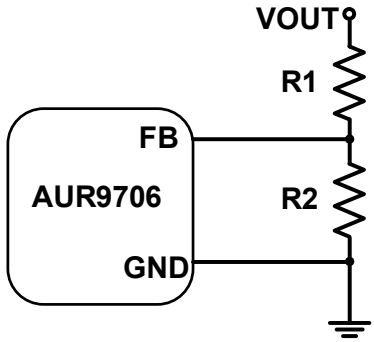


Figure 2. Setting the Output Voltage

Efficiency Considerations

The efficiency of switching regulator is equal to the output power divided by the input power times 100%. It is usually useful to analyze the individual losses to determine what is limiting efficiency and which change could produce the largest improvement. Efficiency can be expressed as:

Efficiency=100%-L1-L2-…where L1, L2,etc. are the individual losses as a percentage of input power. Although all dissipative elements in the regulator produce losses, two major sources usually account for most of the power losses: Vin quiescent current and I^2R losses. The Vin quiescent current loss dominates the efficiency loss at very light load currents but the I^2R loss dominates the efficiency loss at medium to heavy load currents.

1. The V_{IN} quiescent current loss comprises two parts: the DC bias current as given in the electrical characteristics and the internal MOSFET switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each cycle the gate is switched from high to low to high again, the packet of charge ,dQ moves from Vin to ground. The resulting dQ/dt is the current out of V_{IN} that is typically larger than the internal DC bias current. In continuous mode,

$$I_{gate} = f \times (Q_p + Q_n)$$

Where Q_p , Q_n are the gate charge of power PMOSFET and NMOSFET switches. Both the DC bias current and gate charge losses are proportional to the Vin and this effect will be more serious at higher input voltages.

2. I^2R losses are calculated from internal switch resistance, R_{SW} and external inductor resistance RL. In continuous mode, the average output current flowing the inductor is chopped between power PMOSFET switch and NMOSFET switch. Then, the series resistance looking into the LX pin is a function of both PMOSFET and NMOSFET Rds(on) resistance and the duty cycle (D) as follows:
   R_{SW}=[Rds(on)p * D + Rds(on)n * (1-D)
   Therefore, to obtained the I^2R losses, simply add Rsw to RL and multiply the result by the square of the average output current.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2 % of total additional loss.

Thermal Characteristics

In most application, the part does not dissipate much heat due to its high efficiency. But, in some conditions where the part is operating high ambient temperature with high Rds(on) resistance and high duty cycles, such as in LDO mode, the heat dissipated may exceed the maximum junction temperature. To avoid the part from exceeding maximum junction temperature, the user should do some thermal analysis. The maximum power dissipation depends on the layout of PCB , the thermal resistance of IC package, the rate of surrounding airflow and the temperature difference between junction to ambient.

PC Board layout considerations

When laying out the printed circuit board, the following checklist should be used to optimize the performance of AUR9706.

1. The power traces, including the GND trace, the LX trace and the V_{IN} trace should be kept direct, short and wide.
2. Put the input capacitor as close as possible to the Vin and GND pins.
3. The FB pin should be connected directly to the feedback resistor divider.
4. Keep the switching node, LX, away from the sensitive FB pin and the node should be kept small area.
5. The following is an example of 2-layer PCB layout as shown in Figure 4 to Figure 5 for reference.

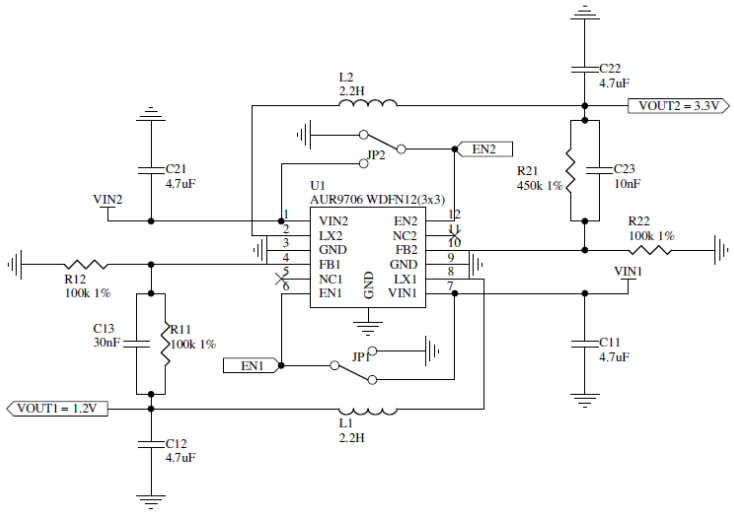


Figure 3. The Evaluation Board Schematic

Evaluation Board Layout

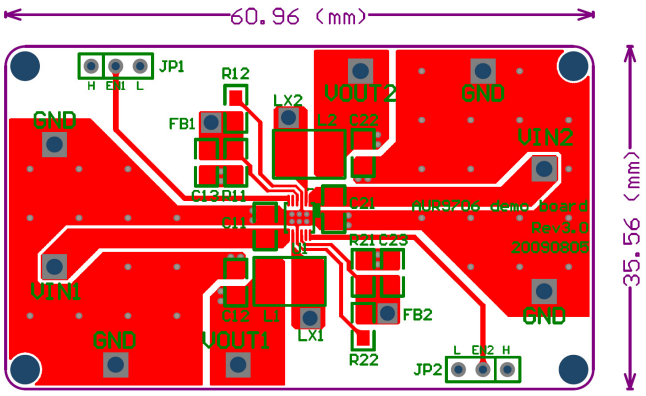


Figure 4. Top Layer Layout

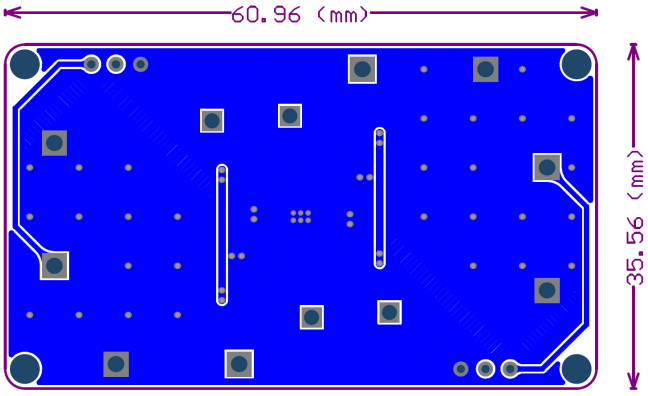
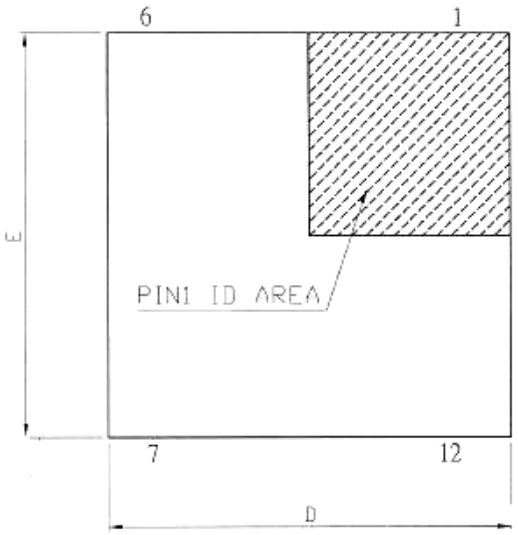
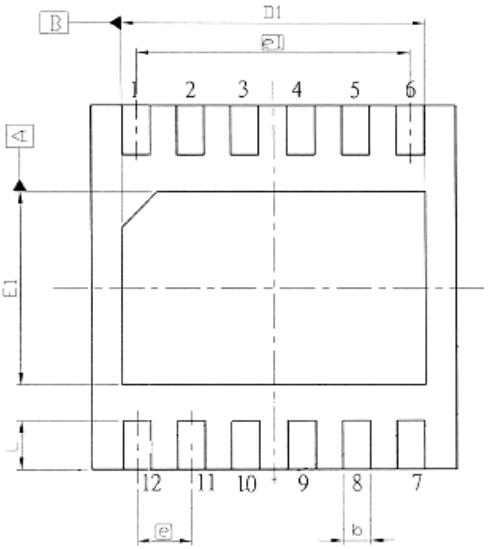
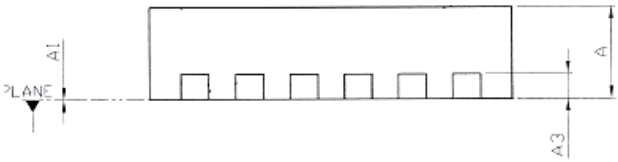


Figure 5. Bottom Layer Layout

Package Information:







SYMBOL	DIMENSION (MM)		DIMENSION (MIL)	
	MIN	MAX	MIN	MAX
A	0.70	0.80	27.6	31.5
A1	0.00	0.05	0.0	2.0
A3	0.203 REF		8 REF	
b	0.18	0.28	7.1	11.0
D	2.95	3.05	116.1	120.1
D1	2.40	2.60	94.5	102.4
E	2.95	3.05	116.1	120.1
E1	1.50	1.70	59.1	66.9
L	0.30	0.50	11.8	19.7
e	0.40	0.50	15.7	19.7
e1	2.20	2.30	86.6	90.6
y	0.00	0.08	0.0	3.0

WDFN-12L 3x3